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Notice of Allowability	Application No.	Applicant(s)	
	10/751,324	MADURAWE, RAMINDA UDAYA	
	Examiner	Art Unit	
	Daniel D. Chang	2819	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.			
1. This communication is responsive to <u>Amendment filed 9/15</u>	<u>5/2006</u> .		
2. 🔀 The allowed claim(s) is/are <u>1-20</u> .			
3.			
Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal P 6. Interview Summary Paper No./Mail Dat 7. Examiner's Amendn 8. Examiner's Stateme 9. Other	(PTO-413), re nent/Comment ent of Reasons for Allo	owance
	,	Daniel D. Chang Primary Examiner Art Unit: 2819	

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Acknowledgement

Receipt is acknowledged of the Amendment filed September 15, 2006.

Reasons for Allowance

Claims 1-20 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: the best prior art of record, Singh et al., taken alone or in combination of other references, does not teach or fairly suggest an integrated circuit comprising, among other things, a second selectable fabrication option comprised of a hard-wired circuit in lieu of said user configurable memory circuit; wherein the IC functionality and performance is substantially identical for a given configuration utilizing the first or second fabrication options (claim 1); a second selectable option comprises a hard-wire read only memory (ROM) construction; wherein, the logic circuits construction comprises one or more masking patterns that are invariant to the memory construction options (claim 8); and a second selectable option comprising a hard-wired read only memory (ROM) construction; wherein the pass-gate logic element construction comprises one or more masking patterns that are invariant to the memory construction options (claim 17), as set forth in the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel D. Chang Primary Examiner

Art Unit 2819

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